IN THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the above-referenced application:

1. (Currently Amended) A metal-oxide-semiconductor (MOS) device, comprising:

a semiconductor layer comprising a substrate of a first conductivity type and a second layer of a second conductivity type formed on at least a portion of the substrate;

a first source/drain region of the second conductivity type formed in the second layer proximate an upper surface of the second layer;

a second source/drain region of the second conductivity type formed in the second layer proximate the upper surface of the second layer and spaced laterally from the first source/drain region;

a gate formed above the second layer proximate the upper surface of the second layer and at least partially between the first and second source/drain regions; and

at least one electrically conductive trench formed in the second layer between the gate and the second source/drain region, the at least one trench being formed proximate the upper surface of the semiconductor layer and extending substantially vertically through the second layer to the substrate;

wherein the at least one trench comprises an insulating material substantially lining sidewalls forming the trench, the trench being substantially filled with an electrically conductive material.

2. (Original) The device of claim 1, wherein the second layer comprises an epitaxial layer.

3. (Original) The device of claim 1, wherein the at least one trench is configured such that as a voltage at the second source/drain region increases, a depletion region spreads from the trench to substantially fill a region proximate the trench, thereby reducing hot carrier injection in the device.

4. (Original) The device of claim 1, further comprising a second electrically conductive trench formed in the second layer between the gate and the second source/drain region, the second trench being formed proximate the upper surface of the semiconductor layer and extending substantially vertically through the second layer to the substrate, the at least first and second trenches being spaced apart relative to one another and configured such that as a voltage at the second source/drain region increases, a depletion region spreads from the trenches to substantially fill a region between the trenches, thereby reducing hot carrier injection in the device.

5. (Original) The device of claim 1, further comprising a shielding structure formed proximate the upper surface of the semiconductor layer and between the gate and the second source/drain region, the shielding structure being electrically connected to the first source/drain region, the shielding structure being spaced laterally from the gate and being substantially non-overlapping relative to the gate.

6. (Original) The device of claim 5, wherein the at least one trench is formed proximate the shielding structure.

7. (Original) The device of claim 1, wherein the at least one trench is substantially filled with an electrically conductive material.

8. (Canceled)

9. (Currently Amended) The device of claim ~~8~~ 1, wherein the insulating material comprises an oxide and the electrically conductive material comprises polysilicon.

10. (Original) The device of claim 1, wherein the device comprises a diffused MOS (DMOS) device.

11. (Original) The device of claim 10, wherein the device comprises a lateral DMOS (LDMOS) device.

12. (Original) The device of claim 1, wherein the first source/drain region comprises a source region and the second source/drain region comprises a drain region.

13. (Original) The device of claim 1, wherein the at least one trench comprises a v-groove.

14. (Original) The device of claim 1, wherein the at least one trench comprises a diffused sinker.

15. (Original) The device of claim 1, further comprising a plurality of electrically conductive trenches formed in the second layer between the gate and the second source/drain region, the trenches being formed proximate the upper surface of the semiconductor layer and extending substantially vertically through the second layer to the substrate, the trenches being spaced apart relative to one another and configured such that as a voltage at the second source/drain region increases, a depletion region spreads from the trenches to substantially fill a region between the trenches, thereby reducing hot carrier injection in the device.

16. (Original) The device of claim 15, wherein the trenches are spaced apart relative to one another and distributed substantially uniformly throughout a region between the gate and second source/drain region.

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Canceled)

22. (Currently Amended) An integrated circuit (IC) device comprising one or more metal-oxide semiconductor (MOS) devices, at least one of the MOS devices comprising:

a semiconductor layer comprising a substrate of a first conductivity type and a second layer of a second conductivity type formed on at least a portion of the substrate;

a first source/drain region of the second conductivity type formed in the second layer proximate an upper surface of the second layer;

a second source/drain region of the second conductivity type formed in the second layer proximate the upper surface of the second layer and spaced laterally from the first source/drain region;

a gate formed above the second layer proximate the upper surface of the second layer and at least partially between the first and second source/drain regions; and

at least one electrically conductive trench formed in the second layer between the gate and the second source/drain region, the at least one trench being formed proximate the upper surface of the semiconductor layer and extending substantially vertically through the second layer to the substrate;

wherein the at least one trench comprises an insulating material substantially lining sidewalls forming the trench, the trench being substantially filled with an electrically conductive material.

23. (Original) The IC device of claim 22, wherein the at least one trench in the at least one MOS device is configured such that as a voltage at the second source/drain region increases, a depletion region spreads from the trench to substantially fill a region proximate the trench, thereby reducing hot carrier injection in the device.

24. (Original) The IC device of claim 22, wherein the at least one MOS device further comprises a second electrically conductive trench formed in the second layer between the gate and the second source/drain region, the second trench being formed proximate the upper surface of the semiconductor layer and extending substantially vertically through the second layer to the substrate, the at least first and second trenches being spaced apart relative to one another and configured such that as a voltage at the second source/drain region increases, a depletion region spreads from the trenches to substantially fill a region between the trenches, thereby reducing hot carrier injection in the device.

25. (Original) The IC device of claim 22, wherein the at least one MOS device further comprises a shielding structure formed proximate the upper surface of the semiconductor layer and between the gate and the second source/drain region, the shielding structure being electrically connected to the first source/drain region, the shielding structure being spaced laterally from the gate and being substantially non-overlapping relative to the gate.

26. (New) The device of claim 4, wherein the at least first and second trenches are spaced apart relative to one another and to a channel region formed in the device between the first and second source/drain regions, the trenches being configured so as to control a curvature of the channel region.

27. (New) The device of claim 1, wherein the insulating material substantially lines all sidewalls forming the at least one trench.

28. (New) The device of claim 22, wherein the insulating material substantially lines all sidewalls forming the at least one trench.

29. (New) A metal-oxide-semiconductor (MOS) device, comprising:

a semiconductor layer comprising a substrate of a first conductivity type and a second layer of a second conductivity type formed on at least a portion of the substrate;

a first source/drain region of the second conductivity type formed in the second layer proximate an upper surface of the second layer;

a second source/drain region of the second conductivity type formed in the second layer proximate the upper surface of the second layer and spaced laterally from the first source/drain region;

a gate formed above the second layer proximate the upper surface of the second layer and at least partially between the first and second source/drain regions; and

a plurality of electrically conductive trenches formed in the second layer between the gate and the second source/drain region, the trenches being formed proximate the upper surface of the semiconductor layer and extending substantially vertically through the second layer to the substrate, the trenches being spaced apart relative to one another and to a channel region formed in the device below at least a portion of the gate and between the first and second source/drain regions, the trenches being configured so as to control a curvature of the channel region.